

REMARKS

I. Introduction

Claims 1 – 14, 16, and 17 are pending in the application. In view of the following remarks, Applicants respectfully request reconsideration of the pending rejections and submit that all pending claims are in condition for allowance.

II. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 1 – 14, 16, and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U.S. Patent No. 6,432,802 to Noda in view of U.S. Patent No. 5,966,623 to Khosla. Applicants traverse this rejection for at least the following reasons.

Claim 1 recites, among other things, forming, after the formation of extension implanted layers, the fluorine implanted layers in the upper portions of the extension implanted layers by implanting fluorine in the semiconductor region using the gate electrode as a mask. The Examiner correctly acknowledges that Noda fails to disclose this feature and relies on Khosla to overcome this deficiency. However, Khosla also fails to disclose at least this feature.

Khosla appears to disclose performing heat treatment in an ambient of non-reactive gases after fluorine or fluorine compound ions are implanted into silicon wafers. Khosla further recites that boron diffusion is beneficially reduced if BF_2 ions are used for boron implantation. Importantly, however, Khosla appears to disclose implanting boron and fluorine at the same time. Therefore, it is impossible for Khosla to teach a structure wherein fluorine is implanted after the implantation of the first impurities, as recited in claim 1.

It is the present inventor who found that fluorine ions in the fluorine implanted layers in the semiconductor region rapidly diffuse in reaction with point defects which may cause transient enhanced diffusion (TED) of impurities during heat treatment, and that this reduces the

number of excessive point defects and suppresses the TED of the impurities, thereby making it possible to form shallow, low-resistance extension diffused layers. No motivation can be found for combining the teachings of Khosla, which only discloses the step of implanting fluorine or fluorine compound ions, with the teachings of Noda, which does not disclose the step of implanting fluorine. In fact, neither reference even acknowledges the problems solved by the present invention.

Moreover, the Examiner alleges that it is obvious to use the gate electrode as a mask during the fluorine implantation since Noda uses the gate electrode as a mask and also that it is obvious to implant fluorine in the upper portions of the implanted layers to reduce diffusion of the first impurities. However, Khosla does not even suggest using the gate electrode as a mask during fluorine implantation and Noda does not disclose implanting fluorine. Thus, there is no suggestion or motivation found in either reference to use the gate electrode as a mask when implanting the fluorine. Furthermore, as described above, Khosla only appears to disclose implanting fluorine and boron at the same time. Thus, it would not have been obvious to implant fluorine in the upper portions of the extension implanted layers to reduce diffusion of the first impurity, as alleged by the Examiner, because Khosla does not teach or suggest forming fluorine implanted layers in the upper portions of the extension implanted layers.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and the combination of Noda and Khosla fails to do so, it is respectfully submitting that claim 1 is patentable over Noda and Khosla taken alone or in combination with one another.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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